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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,713	12/09/2003	Paul Durrant	03226/358001	5463

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OSHA LIANG L.L.P./SUN
1221 MCKINNEY, SUITE 2800
HOUSTON, TX 77010

EXAMINER	
ROSE, HELENE ROBERTA	
ART UNIT	**PAPER NUMBER**
2163	

DATE MAILED: 06/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,713	DURRANT, PAUL	
	Examiner	Art Unit	
	Helene Rose	2163	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-38 have been presented for examination.

2, Claims 1-38 have been rejected.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 5/20/04, accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections – 35 U.S.C 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 7,9,20,31 and 33 are rejected under 112, second paragraph. Claims 7,9,20,31 and 33 recite the following limitation "**or**", this limitation renders the claim vague and indefinite, because the term "**or**" is considered to be alternative language. Therefore, the limitation renders the claim vague and indefinite, because it is unclear as to how the examiner should interpret the claim limitation as it relates to "or".

Claim Rejection – 35 U.S.C – 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Draves et al. (US Patent No. 6,349,355).

Claims 1, 15-16 and 25:

Regarding claims 1, 15-16, and 25, Draves teaches wherein a computer program product comprising program instructions embodied on a media, wherein said instructions, when loaded into a computer system running one or more application programs and an operating system incorporating a kernel, cause the computing system to perform the method of:

providing a privileged mode for executing routines associated with said kernel, and a non-privileged mode for executing routines associated with an application program (column 6, lines 43-47, Draves);

locating the kernel within a first region of memory, and the application program in a second region of memory (Figure 6, all features and column 2, lines 29-39, Draves); and

setting the system to privileged mode in response to accessing code in said first region of memory and to non-privileged mode in response to accessing code in said second region of memory (column 9, lines 37-40, wherein the microprocessor automatically uses different segment registers when operating in the privileged and non-privilege execution modes, accordingly the first segment offset or set of segment offset is active in the non-privilege execution mode and a different segment offset or set of segment offset is active in the privilege execution mode, Draves).

Claims 2, 18 and 26:

Regarding claims 2, 18 and 26, Draves teaches wherein the application program in the second memory region accesses the kernel in the first memory region by making a system call (column 7, lines 45-49, wherein the system function executes from the kernel virtual address space with the user virtual address space being mapped into the kernel address space to allow the kernel to access data from the user space, Draves).

Claims 3 and 27:

Regarding claim 3 and 27, Draves teaches wherein said system call is implemented as a standard function call (column 11, lines 44-50, wherein the system handler of the virtual memory system is configured to switch between a process first address space identifier, i.e. ASID, to its second ASID when switching between the non-privileged execution mode and the privileged execution mode, Draves).

Claims 4 and 28:

Regarding claims 4 and 28, Draves teaches wherein said setting comprises:

switching to privileged mode in response to a function call from the second memory region into the first memory region (column 11, lines 45-50, Draves); and

switching to non-privileged mode in response to a function call from the first memory region into the second memory region (column 11, lines 45-50m wherein the system call handler of the virtual memory system is configured to switch between a process first address space identifier, ASID, to its second ASID when switching between the non-privileged execution mode and the privileged execution mode, results in corresponding switch between the first and second address mappings for a process, Draves).

Claims 5 and 29:

Regarding claims 5 and 29, Draves teaches wherein said setting further comprises reverting to a previous mode at the conclusion of a function call (column 13, lines 63-65, wherein when returning from the kernel to the user process, the processor switches back to the non-privileged execution mode and reverts to the original segment registers, Draves).

Claims 6 and 30:

Regarding claims 6 and 30, Draves teaches wherein said setting further comprises comparing a calling address and a called address for the function call against predetermined address limits to determine in which memory region said calling address and called address are located (Figure 14, all

features and column 11, lines 20-35, wherein The currently active ASID is stored by a processor register, and to translate a specified virtual address, the processor examines entries having the currently valid ASID, and then attempts to find an entry matching, which is equivalent to comparing, the specified virtual address and if such an entry is found, the virtual address is translated using the entry, wherein otherwise, the TLB is updated with the desired entry from the associated databases, Draves).

Claims 7, 20 and 31:

Regarding claims 7, 20 and 31, Draves teaches wherein the computer system memory is divided into pages (column 1, lines 62-65), and the program instructions further cause the computing system to associate an indicator with each page representative of whether the page is located in said first region of memory **or** said second region of memory (column 11, lines 16-20, wherein each translation look-aside buffer, i.e. TLB entry is indexed by and address space identifier, ASID, indicating which user address space is described by the entry, wherein an entry also includes a virtual page number and a corresponding physical page number, Draves).

Claims 8 and 32:

Regarding claims 8 and 32, wherein said indicator is stored in a page translation table (column 11, lines 16-21, wherein an entry also includes a virtual page number corresponding physical page number, and wherein the currently active ASID is stored in the processor register to translate a specified virtual address, Draves).

Claims 9, 21 and 33:

Regarding claims 9, 21, and 33, wherein said indicator has a first value for the second memory region, and a second or third value for said first memory region, and wherein:

code on a page having said first value executes in non-privileged mode and can be accessed from code on a page having said first, second **or** third value (Figure 16, all features, wherein diagram 130, illustrates the first value, i.e. first process ASID and further defined in column 14, lines 1-21,Draves);

code on a page having said second value executes in privileged mode and can be accessed from code on a page having said first, second **or** third value (Figure 16, all features, wherein diagram 130, also describes the second value, i.e. second process ASID, further defined in column 14, lines 1-21,Draves); and

code on a page having said third value executes in privileged mode and can be accessed from code on a page having said second **or** third value (Figure 16, all features, wherein diagram 136, wherein the an ASID is incremented defined the third value, further defined in column 14, lines 1-21,Draves).

Claims 10 and 34:

Regarding claims 10 and 34, wherein a page having said second value is used to reference code routines on one **or** more pages having said third value (column 8, lines 2-8, wherein physical memory is referenced by different virtual addresses depending on whether its is being accessed by the user process or the kernel process and column 14, lines 5-20, wherein first mapping of each pair is identified by the first ASID, while the second mapping of each pair is identified by the second ASID, wherein the two mappings specify the same physical address. However, the virtual address specified by the first mapping corresponds to a virtual page allocated within the user virtual memory space. The virtual address specified by the second mapping corresponds to a virtual page located 1/2 gigabyte below the virtual page allocated within the user virtual memory space and in response to a system call containing a pointer argument, include a step of switching from the non-privileged execution mode to the privileged execution mode, a step consisting of switching the value of the active ASID, which comprises incrementing the current ASID by a value of one and by incrementing by one is equivalent to a third value).

Claims 11, 22 and 35:

Regarding claims 11, 22, and 35, Draves teaches wherein said first memory region is divided into first and second sub-regions, and wherein a function call from the second memory region is permitted into only one of said first and second sub-regions (column 3,lines 22-24, wherein only one address is mapped

into kernel address space at a given time, Draves).

Claims 12 and 36:

Regarding claims 12 and 36, Draves teaches wherein said first and second memory regions are determined as part of system initialization (Figure 5, all features, wherein a system shareable program module such as a DLL is loaded in a range of virtual memory addresses within the address space of the user process, wherein the DLL includes a code portion 25 that remains static during program execution, and a data portion 26 that changes during execution of the program, wherein in Figure 5 illustrates a kernel 24 residing in the upper 2 gigabytes of virtual memory and wherein code must either be loaded at a specific preferred virtual memory address, or be modified to run at some other virtual memory address, and wherein the DLL is configured to execute only in the prescribed range of addresses at which it has been loaded, Draves).

Claims 13, 23 and 37:

Regarding claims 13, 23, and 37, Draves teaches wherein at least a portion of device driver code is located in the second memory region (Figure 6, diagram 39, wherein a multimedia is equivalent to a device driver and column 6, lines 1-18, wherein additional devices are defined, Draves).

Claims 14, 24 and 38:

Regarding claims 14, 24, and 38, Draves teaches wherein at least a portion of trusted application code is located in the first memory region (column 4, lines 60-64, wherein having both privileged and non-privileged modes of execution is equivalent to a trusted application, Draves).

Claim 17:

Regarding claims 17, Draves teaches wherein said access to code in said first region of memory and said access to code in said second region of memory each represents a jump of processing location (Figure 16, diagram 136, wherein increment address space identifier, i.e. ASID, increments, wherein

increment is equivalent to a jump in a process location, Draves).

Claim 19:

Regarding claims 19, wherein the system maintains predetermined address limits for said first and second memory regions, and determines an access to said first and second memory regions by comparing an accessed address with said predetermined address limits (REFER to claim 6, wherein this limitation has already been addressed, Draves).

Prior Art Made of Record

1. Draves et al. (US Patent No. 6,349,355) discloses a computer system has a microprocessor that can execute in a non-privileged user mode and a privileged kernel mode.

2. Oliveri (US Patent No. 7,058,786) discloses a computer having different memory address spaces, wherein a method and system is provided for communicating data.

Point of Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helene Rose whose telephone number is (571) 272-0749. The examiner can normally be reached on 8:00am - 4:30pm Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on (571) 272-1834. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Helene Rose
Technology Center 2100
June 9, 2006

DON WONG
SUPERVISORY PATENT EXAMINER